PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Stephen R. Van Doren, et al.
Serial No.	:	10/760,599
Filing Date	:	January 20, 2004
For	:	SYSTEM AND METHOD TO FACILITATE ORDERING POINT MIGRATION TO MEMORY
Group Art Unit	:	2188
Confirmation No.	:	1105
Examiner	:	Mardochee Chery
Attorney Docket No.	:	200313613-1

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APPEAL BRIEF

Sir:

Pursuant to the Notice of Appeal filed in this case on June 15, 2007, Applicant's representative presents this Appeal Brief.

I. TABLE OF CONTENTS

II. REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, L.P., as indicated by the Assignment recorded January 20, 2004, Reel/Frame: 014919/0101.

III. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

IV. STATUS OF CLAIMS

Claims 1-30 which are attached in Appendix A, are currently pending in this application. Claims 1-4, 9, 14, 16-17, 20, 23-24 and 29 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Pub. No. 2005/0241626 to Glasco ("Glasco"). Claims 5-6, 10-11, 13, 15, 18-19, 21-22, 25-28 and 30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Glasco in view of U.S. Patent Pub. No. 2003/0217236 to Rowlands ("Rowlands"). Claims 7 and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Glasco in view of Rowlands and in further view of U.S. Patent No. 6,138,218 to Arimilli, et al. ("Arimilli"). Claim 8 has been objected to as being dependent from a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The rejection of claims 1-7 and 9-30 is appealed.

V. STATUS OF AMENDMENTS

A Final Office Action ("Final Action") was issued for the present application on March 21, 2007. No amendments were made to the claims after the Final Action.

VI. SUMMARY OF THE CLAIMED SUBJECT MATTER

A. Claim 1

One aspect of the present invention, as recited in claim 1, is directed to a system (10 of FIG. 1) comprising a first node (12 of FIG. 1) that includes an ordering point for data (Par. [0020]). The first node (12 of FIG. 1) is operative to employ a write-back transaction associated with writing the data back to memory (16 of FIG. 1; Par. [0030]). The first node (12 of FIG. 1) broadcasts a write-back message to at least one other node (14 and 20 of FIG. 1) in the system (10 of FIG. 1) in response to an acknowledgement provided by the memory (16 of FIG. 1) indicating that the ordering point for the data has migrated from the first node (10 of FIG. 1) to the memory (16 of FIG. 1; Par. [0031]).

B. Claim 2

Claim 2 is directed to the system (10 of FIG. 1) of claim 1, wherein the first node (12 of FIG. 1) comprises a processor (12 of FIG. 1) having an associated cache (22 of FIG. 1) that comprises a plurality of cache lines (Par. [0023]). One of the plurality of cache lines has an associated state that defines the cache line

as a cache ordering point for the data prior to employing the write-back transaction (Par. [0027]).

C. Claim 3

Claim 3 is directed to the system (10 of FIG. 1) of claim 1, wherein the at least one other node (14 and 20 of FIG. 1) provides a response to the first node (12 of FIG. 1) acknowledging receipt of the write-back message broadcast by the first node (12 of FIG. 1; Par. [0031]).

D. Claim 4

Claim 4 the system (10 of FIG. 1) of claim 3, wherein the first node (12 of FIG. 1) maintains the write-back transaction active until the first node (12 of FIG. 1) receives responses from the at least one other node (14 and 16 of FIG. 1) to the write-back message broadcast by the first node (12 of FIG. 1; Par. [0031]).

E. Claim 5

Claim 5 is directed to the system (10 of FIG. 1) of claim 4, further comprising a third node that issues a source broadcast request for the data employing a source broadcast protocol, the third node retrying the source broadcast request for the data in response to recognizing a conflict associated with the source broadcast request for the data (Par. [0032]).

F. Claim 6

Claim 6 is directed to the system (10 of FIG. 1) of claim 5, wherein the conflict is recognized by the third node in response to one of (i) receiving the write-back message broadcast by the first node (12 of FIG. 1) while the source-broadcast request for the data is active at the third node, or (ii) receiving a conflict response from the first node (12 of FIG. 1) to the source broadcast request issued by the third node (Par. [0032]).

G. Claim 7

Claim 7 is directed to the system of claim 5, wherein the third node retries the source broadcast request employing a forward progress protocol (Par. [0029]).

H. Claim 8

Claim 8 is directed to the system (100 of FIG. 3) of claim 1, wherein the first node (102 of FIG. 3) further comprises a request engine (124 of FIG. 3) having an associated miss address file (126 of FIG. 3; Par. [0056]), the request engine (124 of FIG. 3) allocating an entry in the miss address file (126 of FIG. 3) associated with the write-back transaction for the data that is maintained in the miss address file (126 of FIG. 3) until responses have been received from all other nodes in the system (100 of FIG. 3) to the write-back message broadcast by the first node (102 of FIG. 3; Par. [0060]).

I. Claim 9

Another aspect of the present invention, as recited in claim 9 is directed to a computer system (10 of FIG. 1) comprising a first processor (12 of FIG. 1) that provides a write-back request to transfer an ordering point for desired data from associated cache (22 of FIG. 1) of the first processor (12 of FIG. 1) to memory (16 of FIG. 1; Par. [0030]). The memory (16 of FIG. 1) provides an acknowledgement back to the first processor (12 of FIG. 1) in response to the write-back request (Par. [0030]). The first processor (12 of FIG. 1) provides a source broadcast write-back request to the system (10 of FIG. 1) in response to the acknowledgement provided by the memory (16 of FIG. 1; Par. [0031]). The system (10 of FIG. 1) also comprises at least one other processor (14 of FIG. 1) in the system (10 of FIG. 1) that provides an acknowledgement response to the first processor (10 of FIG. 1) in response to the source broadcast write-back request provided by the first processor (10 of FIG. 1; Par. [0031]).

J. Claim 10

Claim 10 is directed to the system of claim 9, wherein the system (10 of FIG. 1) employs a source broadcast protocol (Par. [0034]). The system (10 of FIG. 1) further comprises a third node that issues a source broadcast request for the desired data, the third node reissuing the request in response to recognizing a conflict associated with the source broadcast request for the desired data (Par. [0032]).

K. Claim 11

Claim 11 is directed to the system (10 of FIG.1) of claim 10, wherein the conflict is recognized by the third node in response to one of (i) receiving the source broadcast write-back request provided by the first node (12 of FIG. 1) while the source-broadcast request for the desired data is active at the third node, or (ii) receiving a conflict response from the first node (12 of FIG. 1) to the source broadcast request issued by the third node (Par. [0032]).

L. Claim 12

Claim 12 is directed to the system (10 of FIG. 1) of claim 10, wherein the third node reissues the request employing a forward progress protocol implemented in the system (Par. [0029]).

M. Claim 13

Claim 13 is directed to the system (100 of FIG. 3) of claim 9, further comprising an entry in a miss address file (126 of FIG. 3; Par. [0056]) at the first processor (102 of FIG. 3) that is associated with transferring the ordering point from the associated cache (114 of FIG.3) of the first processor (102 of FIG. 3) to the memory (110 of FIG. 3). The entry in the miss address file (126 of FIG. 3; Par. [0056]) is maintained until responses to the source broadcast write-back request have been received from all other processors (104 and 106 of FIG. 3) in the system (100 of FIG. 3; Par. [0060]).

N. Claim 14

Claim 14 is directed to the system (10 of FIG. 1) of claim 9, wherein the first processor (12 of FIG. 1) comprises a cache line that contains the desired data in a state that defines the cache line as the ordering point for the desired data prior to issuing the write-back request to the memory (16 of FIG. 1; Par. [0028]).

O. Claim 15

Claim 15 is directed to the system (10 of FIG. 1) of claim 14, wherein the state that defines the cache line as the ordering point for the desired data is selected from a group consisting of a modified state, an owner state and a dirty state, the cache line transitioning to an invalid state after issuing the write-back request to the memory (Par. [0028]).

P. Claim 16

Still another aspect of the invention, as recited in claim 16 is directed to a multiprocessor computer system (10 of FIG. 1, 50 of FIG. 2, 100 of FIG. 3, 160 of FIG. 4, 180 of FIG. 5, 200 of FIG. 6, 220 of FIG. 7, 250 of FIG. 8), comprising means for issuing a write-back request (12 of FIG. 1, 56 of FIG. 2, 102 of FIG. 3, 162 of FIG. 4, 186 of FIG. 5, 208 of FIG. 6, 228 of FIG. 7, 256 of FIG. 8) to migrate an ordering point for data from an associated cache to memory (16 of FIG. 1, 74, 76, 78 and 80 of FIG. 2, 110 of FIG. 3, 168 of FIG. 4, 188 of FIG. 5, 206 of FIG. 6, 226 of FIG. 7, 258 of FIG. 8; Pars. [0030], [0039], [0059], [0063],

[0065], [0068], [0071], [0075]). The system also comprises means for providing (12 of FIG. 1, 56 of FIG. 2, 102 of FIG. 3, 162 of FIG. 4, 186 of FIG. 5, 208 of FIG. 6, 228 of FIG. 7, 256 of FIG. 8) a source broadcast write-back message associated with the data to the system (10 of FIG. 1, 50 of FIG. 2, 100 of FIG. 3, 160 of FIG. 4, 180 of FIG. 5, 200 of FIG. 6, 220 of FIG. 7, 250 of FIG. 8) in response to the memory (16 of FIG. 1, 74, 76, 78 and 80 of FIG. 2, 110 of FIG. 3, 168 of FIG. 4, 188 of FIG. 5, 206 of FIG. 6, 226 of FIG. 7, 258 of FIG. 8) acknowledging receipt of the write-back request (Pars. [0031], [0041], [0060], [0064], [0065], [0068], [0071], [0075]).

Q. Claim 17

Claim 17 is directed to the system (10 of FIG. 1, 50 of FIG. 2, 100 of FIG. 3, 160 of FIG. 4, 180 of FIG. 5, 200 of FIG. 6, 220 of FIG. 7, 250 of FIG. 8) of claim 16, further comprising means at each of at least one node (14 and 20 of FIG. 1, 54, 58, 60 and 82 of FIG. 2, 104 and 106 of FIG. 3, 164 and 166 of FIG. 4, 182 and 184 of FIG. 5, 204 and 212 of FIG. 6, 222 and 224 of FIG. 7, 252 and 254 of FIG. 8) in the system (10 of FIG. 1, 50 of FIG. 2, 100 of FIG. 3, 160 of FIG. 4, 180 of FIG. 5, 200 of FIG. 6, 220 of FIG. 7, 250 of FIG. 8) for acknowledging receipt of the source broadcast write-back message (Pars. [0031], [0041], [0060], [0064], [0065], [0068], [0071]).

R. Claim 18

Claim 18 is directed to the system (10 of FIG. 1, 50 of FIG. 2, 100 of FIG. 3, 160 of FIG. 4, 180 of FIG. 5, 200 of FIG. 6, 220 of FIG. 7, 250 of FIG. 8) of claim 17, further comprising means for retiring (12 of FIG. 1, 56 of FIG. 2, 102 of FIG. 3, 162 of FIG. 4, 186 of FIG. 5, 208 of FIG. 6, 228 of FIG. 7, 256 of FIG. 8) an outstanding transaction associated with migration of the ordering point to the memory (16 of FIG. 1, 74, 76, 78 and 80 of FIG. 2, 110 of FIG. 3, 168 of FIG. 4, 188 of FIG. 5, 206 of FIG. 6, 226 of FIG. 7, 258 of FIG. 8) from the associated cache (22 of FIG. 1, 66 of FIG. 2, 114 of FIG. 3) in response to receiving acknowledgement of receipt of the source broadcast write-back message (Pars. [0031], [0041], [0060], [0064], [0065], [0068], [0071]).

S. Claim 19

Claim 19 is directed to the system (10 of FIG. 1, 50 of FIG. 2, 100 of FIG. 3, 160 of FIG. 4, 180 of FIG. 5, 200 of FIG. 6, 220 of FIG. 7, 250 of FIG. 8) of claim 16, further comprising means for recognizing a conflict (12, 14 and 20 of FIG. 1, 54, 56, 58, 60 and 82 of FIG. 2, 102, 104 and 106 of FIG. 3, 162, 164 and 166 of FIG. 4, 182 of FIG. 5, 224 of FIG. 7, 252 of FIG. 8) associated with the data (Pars. [0032], [0041], [0061], [0064], [0066], [0071], [0076]).

T. Claim 20

Claim 20 is directed to the system (10 of FIG. 1, 50 of FIG. 2, 100 of FIG. 3, 160 of FIG. 4, 180 of FIG. 5, 200 of FIG. 6, 220 of FIG. 7, 250 of FIG. 8)

of claim 16, wherein the means for issuing (12 of FIG. 1, 56 of FIG. 2, 102 of FIG. 3, 162 of FIG. 4, 186 of FIG. 5, 208 of FIG. 6, 228 of FIG. 7, 256 of FIG. 8) the write-back request comprises a first processor (12 of FIG. 1, 56 of FIG. 2, 102 of FIG. 3) including a cache line that contains the data in a state that defines the cache line as the ordering point for the data prior to migration of the ordering point to the memory (16 of FIG. 1, 74, 76, 78 and 80 of FIG. 2, 110 of FIG. 3, 168 of FIG. 4, 188 of FIG. 5, 206 of FIG. 6, 226 of FIG. 7, 258 of FIG. 8; Pars. [0028], [0039], [0059]).

U. Claim 21

Claim 21 is directed to the system (10 of FIG. 1, 50 of FIG. 2, 100 of FIG. 3, 160 of FIG. 4, 180 of FIG. 5, 200 of FIG. 6, 220 of FIG. 7, 250 of FIG. 8) of claim 20, wherein the state that defines the cache line as the ordering point for the data is selected from a group consisting of a modified state, an owner state and a dirty state, the cache line transitioning to an invalid state after issuing the write-back request to the memory (16 of FIG. 1, 74, 76, 78 and 80 of FIG. 2, 110 of FIG. 3, 168 of FIG. 4, 188 of FIG. 5, 206 of FIG. 6, 226 of FIG. 7, 258 of FIG. 8; Pars. [0028], [0039], [0059]).

V. Claim 22

Claim 22 is directed to the system (10 of FIG. 1, 50 of FIG. 2, 100 of FIG. 3, 160 of FIG. 4, 180 of FIG. 5, 200 of FIG. 6, 220 of FIG. 7, 250 of FIG. 8) of claim 16, further comprising means for transitioning (12 of FIG. 1, 56 of FIG. 2,

102 of FIG. 3) a cache line in the associated cache to an invalid cache state for the data after the write-back request is issued (Pars. [0028], [0039], [0059]).

W. Claim 23

Still yet another aspect of the invention, as recited in claim 23 is directed to a method comprising providing a write-back request (300 of FIG. 9) from a first processor node to transfer an ordering point associated with data to memory (Par. [0077]). The method also comprises acknowledging receipt (310 of FIG. 9) of the write back request at the memory (Par. [0077]). The method further comprises issuing a source broadcast message (320 of FIG. 9) from the first processor node to other nodes in response to the acknowledging receipt of the write back request at the memory (Par. [0077]).

X. Claim 24

Claim 24 is directed to the method of claim 23, further comprising providing a response from each of the other nodes (14 and 20 of FIG. 1) to acknowledge receipt of the source broadcast message at the other nodes (14 and 20 of FIG. 1; Par. [0031]).

Y. Claim 25

Claim 25 the method of claim 24, further comprising maintaining a write-back transaction at the first processor node (12 of FIG. 1) until the first processor node (12 of FIG. 1) receives the responses to the source broadcast message from the other nodes (Par. [0031]).

Z. Claim 26

Claim 26 is directed to the method of claim 25, further comprising retiring the write-back transaction at the first processor node (12 of FIG. 1) in response to receiving the responses from each of the other nodes (14 and 20 of FIG. 1) acknowledging receipt of the source broadcast message (Par. [0031]).

AA. Claim 27

Claim 27 is directed to the method of claim 23, further comprising recognizing a conflict associated with a request for the data provided by at least one of the other nodes (14 and 20 of FIG. 1; Par. [0032]).

AB. Claim 28

Claim 28 is directed to the method of claim 27, wherein the request for the data provided by the at least one of the other nodes (14 and 20 of FIG. 1) comprises a source broadcast request (Par. [0032]) The recognizing of the conflict further comprising recognizing the conflict in response to one of (i) receiving the source broadcast write-back request provided by the first processor node (12 of FIG. 1) while the source-broadcast request for the data is outstanding at the at least one of the other nodes (14 and 20 of FIG. 1), or (ii) receiving a conflict response from the first node to a source broadcast request issued by the at least one of the other nodes (14 and 20 of FIG. 1; Par. [0032]).

AC. Claim 29

Claim 29 is directed to the method of claim 23, wherein the first processor (12 of FIG. 1) comprises a cache line that contains the data in a state that defines the cache line as the ordering point for the data prior to issuing the write-back request to the memory (16 of FIG. 1; Par. [0028]).

AD. Claim 30

Claim 30 is directed to the method of claim 29, further comprising transitioning the state of the data in the first processor (12 of FIG. 1) from a first state to an invalid state after issuing the write-back request to the memory (16 of FIG. 1), the first state being selected from a group consisting of a modified state, an owner state and a dirty state (Par. [0028]).

VII. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1-4, 9, 14, 16-17, 20, 23-24 and 29 are anticipated by Glasco.

B. Whether claims 5-6, 8, 10-11, 13, 15, 18-19, 21-22, 25-28 and 30 are made obvious by Glasco in view of Rowlands.

C. Whether claims 7 and 12 are made obvious by Glasco in view of Rowlands and in further view of Arimilli.

VIII. ARGUMENT

A. 35 U.S.C. §102(e) rejection of claims 1-4, 9, 14, 16-17, 20, 23-24 and 29 as being anticipated by Glasco

Anticipation by a single reference requires that the single prior art reference disclose each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984).

1. The Anticipation Rejection of Claim 1

Glasco does not anticipate the system of claim 1. Claim 1 recites a system where a first node, which includes an ordering point for data, employs a write-back transaction associated with writing the data back to memory. Claim 1 also recites that the memory provides an acknowledgement to indicate that the ordering point for the data has migrated to the memory. Generally stated, in claim 1, the ordering point for the data migrates from the first node to the memory and the memory provides an acknowledgement to indicate that such ordering point migration has occurred.

Glasco does not disclose that an ordering point can migrate from a node to memory, as recited in claim 1. Instead, Glasco employs memory controllers to act as serialization points for each memory line, but fails to disclose that any

serialization point for a memory line can migrate (See Glasco, Pars. [0047] and [0127]).

It is argued in the Final Action that since Glasco discloses a cache writing a line back to memory that Glasco must disclose migrating an ordering point for a given cache line from a cache to memory, as recited in claim 1 (See Final Action, Pages 3-4). To support this statement, the Final Action has cited Paragraph [0028] of the present application's specification. Applicant's representative respectfully submits that the Final Action is attempting to impermissibly use the particular implementation details of the system disclosed in the present application to reject claim 1. Applicant's representative respectfully submits that the present Application (and particularly not Paragraph [0028] of the present application) does not qualify as prior art under 35 U.S.C. §102(e) to support an anticipation rejection of claim 1.

Moreover, in Glasco, even during an eviction or write transaction, such as during a write back to memory, a given memory controller remains the serialization point for the memory line before, during and after writing back to memory (See Glasco Pars. [0137] and [0127]). Since Glasco fails to disclose that an ordering point can migrate from a node to memory, as recited in claim 1, Glasco consequently also fails to disclose that memory would provide any acknowledgement to indicate that the ordering point has migrated from the first node to the memory, as recited in claim 1.

Applicant's representative respectfully submits that claim 1 has been mischaracterized. In the Final Action, it is alleged that Glasco's disclosure of "sending invalidation messages to each of the remote caches in a cluster system if a directory indicates that the line is in the dirty state and the modified line must be written back to memory" reads on the acknowledgement indicating that the ordering point has migrated from a node to memory, as recited in claim 1 (See Final Action, Page 5). However, once again, the Final Action has impermissibly relied on the present application's specification to support this contention. Furthermore, providing invalidation messages, as disclosed in Glasco, does not appear to have any relationship to the ordering point for a cache line, in contrast to the contentions of the Final Action.

Additionally, the Final Action appears to have misconstrued the teachings of Glasco by contending that the modified write back message described in Glasco is provided in response to an acknowledgement provided by the memory indicating that the ordering point has migrated from the first node to the memory. In contrast to the contentions made in the Final Action, Glasco discloses that a modified line of memory must first be written back to memory before the line is invalidated if the directory entry indicates that the line is in the "dirty" state in any of the remote caches (See Glasco, Par. [0116] at Lines 4 to 8, and Par. [0126]). As discussed above, however, Glasco fails to disclose that an ordering point migrates for data write-backs to memory. Consequently, Glasco cannot disclose

broadcasting of a write-back message by the first node in response to the acknowledgement provided by the memory, as recited in claim 1. For the reasons stated above, Glasco fails to anticipate claim 1. Thus, Applicant's representative respectfully requests that the rejection of claim 1 be withdrawn.

2. The Anticipation Rejection of Claim 2

Claim 2 depends from claim 1 and is not anticipated by Glasco for at least the same reasons as claim 1, and for the following reasons. Glasco fails to disclose that a cache lines has an associated state that defines the cache line as a cache ordering point for the data prior to employing the write-back transaction (of claim 1), as recited in claim 2. As discussed with respect to claim 1, Glasco discloses that a memory controller acts as a serialization point for a memory line (See Glasco Pars. [0045]-[0046]), but fails to disclose that an associated state of a cache line defines the cache line as an ordering point for the data, as recited in claim 2. This is because the memory controller in Glasco operates as the serialization point regardless of the state of a given cache line.

Moreover, it is contended in the Final Action that Paragraph [0126] of Glasco discloses the elements recited in claim 2. However, Paragraph [0126] of Glasco actually supports Applicant's position since the cited section of Glasco discloses that the home memory controller is a serialization point. Therefore Glasco fails to disclose the elements recited in claim 2.

In the Final Action, it is argued that since Glasco discloses a cache writing a line back to memory that Glasco must disclose migrating an ordering point for a given cache line from a cache to memory (See Final Action, Page 8). To support this statement, the Final Action has cited Paragraph [0028] of the present application's specification. Applicant's representative respectfully submits that the Final Action is attempting to impermissibly use the particular implementation details of the system disclosed in the present application to reject claim 2. Applicant's representative respectfully submits that the present application does not qualify as prior art under 35 U.S.C. §102(e) to support an anticipation rejection of claim 2. Thus, Glasco does not anticipate claim 2. Accordingly, Applicant's representative respectfully requests that the rejection of claim 2 be withdrawn.

3. <u>The Anticipation Rejection of Claim 3</u>

Claim 3 depends from claim 1 and is not anticipated for at least the same reasons as claim 1 and for the following reasons. Glasco fails to disclose that at least one other node provides a response to the first node acknowledging receipt of the write-back message broadcast by the first node, as recited in claim 3. Instead, Glasco discloses that a home memory controller receives a dirty copy of the memory line, writes the line back to memory and notifies the originator of the transaction that the transaction is complete (See Glasco, Par. [0126]). However,

in Glasco, the originator of the transaction (the cache coherence controller in the home cluster - see Glasco Par. [0124]) does not broadcast a write back message, as recited in claim 1, from which claim 3 depends. Instead, in Glasco a home memory controller notifies the cache directory that the transaction is complete (See Glasco, Par. [0126]). Therefore, in Glasco, the notification is not disclosed as being provided for acknowledging a write-back message that was broadcast by a first node, in contrast to the system recited in claim 3. For these reasons, Glasco does not anticipate claim 3. Accordingly, Applicant's representative respectfully requests withdrawal of the rejection of claim 3.

4. The Anticipation Rejection of Claim 4

Claim 4 depends from claims 3 and 1 and is not anticipated for at least the same reasons as claims 3 and 1 and for the following reasons. In the Final Action, Paragraphs [0121]-[0123] and [0127] are cited to support a contention that Glasco discloses claim 4. However, nothing in the cited sections of Glasco or elsewhere in Glasco is there a disclosure that the first node (which employs the write back transaction - of claim 1) maintains the transaction active until such first node receives responses from the at least one other node to the write-back message that was broadcast by the first node, as recited in claim 4. Rather, Glasco discloses that once a memory controller accepts a sized write transaction, the memory controller does not allow any further transactions for the

same memory line until the eviction process is complete (See Glasco, Par. [0127]).

Moreover, Applicant's representative submits that there is no discussion in the Final Action as to what parts of Glasco might correspond to claimed subject matter. The sections of Glasco being relied upon fail to disclose that any message or notification is broadcast by the originator of the transaction (the cache coherence controller). The Final Action argues that such an element is not claimed in claim 4 (See Final Action, Page 9). Applicant's representative respectfully disagrees. Claim 1, from which claim 4 depends, recites broadcasting a write-back message to at least one other node in a system in response to an acknowledgement provided by the memory. Thus, by virtue of claim 4's dependence from claim 1, claim 4 recites broadcasting a write-back message. Thus, Glasco does not anticipate claim 4. Accordingly, Applicant's representative respectfully requests that the rejection of claim 4 be withdrawn.

5. <u>The Anticipation Rejection of Claim 9</u>

In the Final Action, it is contended that Glasco discloses the system of claim 9 for the same reasons as the rejections of claims 1 and 2 (See Final Action, Page 14). Applicant's representative respectfully disagrees with this contention. Glasco does not disclose a first processor that provides a write-back request to transfer an ordering point for desired data from an associated cache of

the first processor to memory, as recited in claim 9. Instead, in Glasco, the ordering point for a line of memory remains in the memory controller - before, during and after the memory line is written back to memory (See Glasco, Pars. [0127] and [0137]). Consequently, Glasco also fails to disclose the other acknowledgement and broadcasting of requests that occur in response to the write-back request provided by the first processor, as recited in claim 9. Therefore, Glasco does not disclose each and every element of claim 9.

For the reasons described above, Glasco does not anticipate claim 9. Accordingly, Applicant's representative respectfully requests that the rejection of claim 9 be withdrawn.

6. The Anticipation Rejection of Claim 14

Claim 14 depends from claim 9 and is not anticipated for at least the same reasons as claim 9, and for the following reasons. Glasco fails to disclose a cache line that contains desired data in a state that defines the cache line as the ordering point for the desired data prior to issuing the write-back request to memory. Glasco discloses that a memory controller acts as a serialization point for a memory line (see Glasco Pars. [0045]-[0046]), but fails to disclose that an associated state of a cache line defines the cache line as an ordering point for the data, as recited in claim 14. That is, the memory controller in Glasco remains the serialization point for a given cache line for ordering requests for the given

cache line regardless of its state. Thus, Glasco does not anticipate claim 14. Therefore, Applicant's representative respectfully requests that the rejection of claim 14 be withdrawn.

7. The Anticipation Rejection of Claim 16

Glasco does not anticipate claim 16. Glasco does not disclose means for issuing a write-back request to migrate an ordering point for data from an associated cache to memory. Instead, Glasco discloses that a home memory controller acting as the serialization point receives a "dirty" copy of the memory line, and writes the line back to memory (See Glasco, Par. [0126]). The write-back disclosed in Glasco transfers a memory line to memory, but fails to disclose migration of an ordering point from an associated cache to memory, as recited in claim 16. Therefore, Glasco does not anticipate claim 16. Accordingly, Applicant's representative respectfully requests that the rejection of claim 16 be withdrawn.

8. The Anticipation Rejection of claims 17 and 20

Claims 17 and 20 depend from claim 16 and are not anticipated for at least the same reasons as claim 16 and for the specific elements recited therein. Accordingly, the rejection of claims 17 and 20 should be withdrawn.

9. The Anticipation Rejection of Claim 23

Glasco fails to anticipate claim 23. The system of Glasco fails to disclose that a write-back request from a first processor node is provided to transfer an ordering point to memory, in contrast to the method recited in claim 23. Moreover, there is no basis to conclude that Glasco discloses that the originator of the write back (the first processor node) also provides a source broadcast message to other nodes in response to an acknowledging receipt of the write-back request at the memory, as recited in claim 23. Instead, the system in Glasco issues probes from the home memory controller in response to the originating sized write request, in response to which the local nodes respond by returning any dirty copy of the memory line and invalidating the corresponding entries in their caches (See Glasco, Pars. [0124]-[0125]). Accordingly, Glasco does not anticipate claim 23. Therefore, withdrawal of the rejection of claim 23 is respectfully requested.

10. The Anticipation Rejection of Claim 24

Claim 24 depends from claim 23 and is not anticipated for at least the same reasons as claim 23 and for the following reasons. Glasco fails to disclose providing a response from each of the other nodes to acknowledge receipt of the source broadcast message at the other nodes, as recited in claim 24. Instead,

Glasco discloses that a home memory controller receives a dirty copy of the memory line, writes the line back to memory and notifies the originator of the transaction that the transaction is complete (See Glasco Par. [0126]). However, in Glasco, the originator of the transaction does not broadcast a write back message, as recited in claim 23, from which claim 24 depends. Therefore, Glasco cannot disclose providing a response from each of the other nodes to acknowledge receipt of the source broadcast message at the other nodes, as recited in claim 24, since in Glasco, no source broadcast message is disclosed. Thus, Glasco does not anticipate claim 24, and withdrawal of the rejection of claim 24 is respectfully requested.

11. <u>The Anticipation Rejection of Claim 29</u>

Claim 29 depends from claim 23 and is not anticipated by Glasco for at least the same reasons as claim 23, and for the following reasons. Glasco fails to disclose a processor that comprises cache lines that contains data in a state that defines a cache line as the ordering point for the data prior to issuing the write-back request to the memory, as recited in claim 29. Glasco discloses that a memory controller acts as a serialization point for a memory line (see Glasco Pars. [0045]-[0046]), but fails to disclose that an associated state of a cache line defines the cache line as an ordering point for the data, as recited in claim 29.

Therefore, Glasco does not anticipate claim 29. Thus, Applicant's representative respectfully requests that the rejection of claim 29 be withdrawn.

B. 35 U.S.C. §103(a) Rejection of Claims 5-6, 8, 10-11, 13, 15, 18-19, 21-22, 25-28 as being Made Obvious by Glasco in view of Rowlands

Obviousness requires a suggestion of all limitations in a claim. *CFMT, Inc. v. YieldUp Int'l Corp.*, 349 F.3d 1333, 1342, 68 U.S.P.Q.2d 1940 (Fed. Cir. 2003).

1. The Obviousness Rejection of Claim 5

Claim 5 depends from claim 1 and is patentable for at least the same reasons as claim 1. Moreover, the addition of Rowlands does not make up for the aforementioned deficiencies of Glasco with respect to claim 1.

Additionally, it is contended in the Final Action that Rowlands teaches the elements recited in claim 5 (See Final Action, Page 16, citing Rowlands, Pars. [0057] and [0113]). Applicant's representative respectfully submits that Glasco taken in view of Rowlands fails to teach or suggest that a transaction would be retried in response to recognizing a conflict, as recited in claim 5. Instead, the cited section of Rowlands simply discloses an interconnect that may or may not support retry of an address transfer (See Rowlands, Par. [0113]). Thus, Glasco and Rowlands, taken individually or in combination fail to provide sufficient motivation to create the system of claim 5. Accordingly, Glasco taken

in view of Rowlands does not make claim 5 obvious, and withdrawal of the rejection of claim 5 is respectfully requested.

2. The Obviousness Rejection of Claim 6

Claim 6 depends from claim 5. Accordingly, claim 6 is not made obvious by Glasco taken in view of Rowlands for at least the same reasons as claim 5, and for the following reasons.

The Final Action contends that Paragraph [0127] of Glasco teaches the elements of claim 6 (See Final Action, Page 16). However, this section of Glasco has no teaching or suggestion that any third node can recognize a conflict, as recited in claim 6. Instead, Paragraph [0127] of Glasco describes some particular functionality of a home memory controller and the role it plays in avoiding race conditions during a write back of a memory line (See Glasco, Par. [0127]).

In the Final Action, it is argued that Glasco discloses that conflicting transactions may be generated (See Final Action, Page 11). However, even assuming *arguendo* that this is true, the Final Action fails to cite any section of Glasco or Rowlands that teaches or suggests a conflict being recognized by a third node, as recited in claim 6. Thus, Glasco taken in view of Rowlands fails to make claim 6 obvious, and the rejection of claim 6 should be withdrawn.

3. The Obviousness Rejection of Claim 10

Claim 10 depends from claim 9 and is patentable for at least the same reasons as claim 9. Moreover, the addition of Rowlands does not make up for the aforementioned deficiencies of Glasco with respect to claim 9.

Additionally, the Final Action alleges that Rowlands teaches the elements recited in claim 10 (See Final Action, Page 17, citing the rejection of claim 5). Applicant's representative respectfully submits that Glasco taken in view of Rowlands fails to teach or suggest that a third node issues a source broadcast request for the desired data and such third node reissues the request in response to recognizing a conflict associated with the source broadcast request for the desired data, as recited in claim 10. Instead, Rowlands simply discloses an interconnect that may or may not support a retry of an address transfer (See Rowlands, Par. [0113]). Such general teaching does not amount to a teaching that a retry would occur under the specific conditions recited in the system of claim 10. Thus, Glasco and Rowlands, taken individually or in combination fail to provide sufficient motivation to create the system of claim 10. Accordingly, Glasco taken in view of Rowlands does not make claim 10 obvious, and withdrawal of the rejection of claim 10 is respectfully requested.

4. The Obviousness Rejection of Claim 11

Claim 11 depends from claim 10. Accordingly, claim 11 is not made obvious by Glasco taken in view of Rowlands for at least the same reasons as claim 10, and for the following reasons.

The Final Action contends that Paragraph [0127] of Glasco teaches the elements of claim 11 (See Final Action, Page 17, citing the rejection of claim 6). However, the cited section of Glasco has no teaching or suggestion that any third node can recognize a conflict in response to the conditions recited in claim 11. Instead, Paragraph [0127] of Glasco describes some particular functionality of a home memory controller and the role it plays in avoiding race conditions during a write back of a memory line (See Glasco, Par. [0127]). Thus, Glasco taken in view of Rowlands fails to make claim 11 obvious, and the rejection of claim 11 should be withdrawn.

5. The Obviousness Rejection of Claim 13

The Final Action has failed to establish a prima facie case of obviousness with respect to claim 13. In rejecting claim 13, the Final Action relies solely on the rejection of claim 8 (See Final Action, Page 17). However, claim 8 was indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims (See Final Action, Page

19). Accordingly, it appears that the rejection of claim 13 was made in error. Thus, the rejection of claim 13 should be withdrawn.

6. The Obviousness Rejection of Claims 15 and 21

Claims 15 and 21 depend from claims 14 and 20, respectively. Accordingly, claims 15 and 21 are patentable for at least the same reasons as claims 14 and 20. The addition of Rowlands does not make up for the aforementioned deficiencies of Glasco with respect to claims 14 and 20.

Additionally, in the Final Action, it is contended that Glasco teaches the elements recited in claims 15 and 21 (See Final Action, Pages 17 and 18). Applicant's representative respectfully disagrees. Glasco fails to teach or suggest that a state of a cache line can define a cache line as an ordering point, as recited in claims 15 and 21. Instead, Glasco teaches that the serialization point (memory controller or a cache controller) for a memory line is independent of the state of a given line of memory (See Glasco Pars. [0045]-[0046], [0127] and [0137]). Therefore, Glasco taken in view of Rowlands does not make claims 15 and 21 obvious. Accordingly, Applicant's representative respectfully requests that the rejection of claims 15 and 21 be withdrawn.

7. The Obviousness Rejection of Claim 18

Claim 18 depends from claim 17 and is patentable for at least the same reasons as claim 17. The addition of Rowlands does not make up for the aforementioned deficiencies of Glasco with respect to claim 17.

Additionally, it is contended that Rowlands teaches the elements recited in claim 18 (See Final Action, Page 16, citing Rowlands, Pars. [0057], [0065] and [0113]). Applicant's representative respectfully submits that in the rejection of claim 18, claim 18 has been mischaracterized. Specifically, the Final Action states that claim 18 recites "means for retrying..," while claim 18 actually recites "means for retiring..." Moreover, Glasco taken in view of Rowlands fails to teach or suggest means for retiring an transaction associated with migration of an ordering point to a memory from an associated cache in response to receiving acknowledgement of receipt of a source broadcast write-back message, as recited in claim 18. Instead, Rowlands simply discloses an interconnect that may or may not support retry of an address transfer (See Rowlands, Par. [0113]). Thus, Glasco and Rowlands, taken individually or in combination fail to provide sufficient motivation to create the system of claim 18. Accordingly, Glasco taken in view of Rowlands does not make claim 18 obvious, and the rejection of claim 18 should be withdrawn.

8. The Obviousness Rejection of Claim 19

Claim 19 depends from claim 16 and is patentable for at least the same reasons as claim 16. The addition of Rowlands does not make up for the aforementioned deficiencies of Glasco with respect to claim 16.

Additionally, the Final Action contends that Rowlands teaches the elements recited in claim 19 (See Final Action, Page 16, citing the rejection of claim 5). Applicant's representative respectfully submits that Glasco taken in view of Rowlands fails to teach or suggest means for recognizing a conflict associated with data, as recited in claim 19. Instead, Rowlands simply discloses an interconnect that may or may not support retry of an address transfer (See Rowlands, Par. [0113]). As discussed herein, Glasco fails to disclose or suggest any mechanism to recognize conflicts under the conditions recited in claim19. Thus, Glasco and Rowlands, taken individually or in combination fail to provide sufficient motivation to create the system of claim 19.

9. The Obviousness Rejection of Claim 22

Claim 22 depends from claim 16 and is patentable for at least the same reasons as claim 16. The addition of Rowlands does not make up for the aforementioned deficiencies of Glasco with respect to claim 16. Accordingly, Glasco taken in view of Rowlands does not make claim 22 obvious. Therefore, the rejection of claim 22 should be withdrawn.

10. The Obviousness Rejection of Claims 25 and 26

Claims 25 and 26 depend from claim 24 and are patentable for at least the same reasons as claim 24. The addition of Rowlands does not make up for the aforementioned deficiencies of Glasco with respect to claim 24.

Additionally, the rationale relied upon in the Final Action (the same rationale as applied to claim 5) fails to establish a prima facie case of obviousness with respect to claims 25 and 26. In particular, since claim 5 does not recite the same subject matter as claim 25 (e.g., maintaining a write-back transaction..., as recited in claim 25, or retiring a write-back transaction..., as recited in claim 26), the incorporation of the rationale provided in the Final Action is an insufficient basis for the rejection of claims 25 and 26. Accordingly, the rejection of claims 25 and 26 should be withdrawn.

11. The Obviousness Rejection of Claim 27

Claim 27 depends from claim 23 and is patentable for at least the same reasons as claim 23. The addition of Rowlands does not make up for the aforementioned deficiencies of Glasco with respect to claim 23.

Additionally, the Final Action contends that Rowlands teaches the elements recited in claim 27 (See Final Action, Page 18, citing the rejection of claim 5). Applicant's representative respectfully submits that Glasco taken in

view of Rowlands fails to teach or suggest any structure programmed or configured for recognizing a conflict associated with a request for data provided by at least one of the other nodes, as recited in claim 27. Instead, Rowlands simply discloses an interconnect that may or may not support retry of an address transfer (See Rowlands, Par. [0113]). Thus, Glasco and Rowlands, taken individually or in combination fail to provide sufficient motivation to create the method of claim 27.

12. The Obviousness Rejection of Claim 28

Claim 28 depends from claim 27. Accordingly, claim 28 is not made obvious by Glasco taken in view of Rowlands for at least the same reasons as claim 27, and for the following reasons.

The Final Action contends that Glasco teaches the elements of claim 28 (See Final Action, Page 18, citing the rejection of claim 6). However, Glasco has no teaching or suggestion that any other node can recognize a conflict in response to the conditions recited in claim 28. Instead, Paragraph [0127] of Glasco describes some particular functionality of a home memory controller and the role it plays in avoiding race conditions during a write back of a memory line (See Glasco, Par. [0127]). Thus, Glasco taken in view of Rowlands fails to make claim 28 obvious, and the rejection of claim 28 should be withdrawn.

13. The Obviousness Rejection of Claim 30

Claim 30 depends from claims 29 and 23. Accordingly, claim 30 is patentable for at least the same reasons as claims 29 and 23. Moreover, the addition of Rowlands does not make up for the aforementioned deficiencies of Glasco with respect to claims 29 and 23. Accordingly, Glasco taken in view of Rowlands does not make claim 30 obvious, and Applicant's representative respectfully requests that the rejection of claim 30 be withdrawn.

C. 35 U.S.C. §103(a) rejection of Claims 7 and 12 as being unpatentable over Glasco in view of Rowlands and further in view of Arimilli

Claims 7 and 12 depend from claims 5 and 10, respectively, and are patentable for at least the same reasons as claims 5 and 10. Moreover, the further addition of Arimilli does not make up for the deficiencies of Glasco taken in view of Rowlands as applied to claims 5 and 10 from which claims 7 and 12 respectively depend. In contrast to the allegations in the Final Action, the approach taught by Arimilli is not that a given node retries its own source broadcast request employing a forward progress protocol, as recited in claims 7 and 12. Instead, Arimilli teaches that a responding cache 114 takes action, such as altering the coherency state associated with requested cache item 208 in its own memory or initiating a push operation to write (modified) requested cache

item 208 to system memory (See Arimilli at Col. 5, lines 32-51, and Abstract). That is, in Arimilli, the cache 116 that issues the retry 206 does not retry its transaction using any forward progress protocol, but instead it is the responding cache 114 that initiates the action to enable an intervention response to proceed (See Arimilli, Col. 5, lines 32-51). Such actions, however, fail to correspond to a retry of the source broadcast request by employing a forward progress protocol since, in the approach taught by Arimilli, no request is retried during such intervention. For at least these reasons, Applicant's representative respectfully submits that Glasco taken in view of Rowlands and in further view of Arimilli fails to make claims 7 and 12 obvious. Accordingly, withdrawal of the rejection of claims 7 and 12 is respectfully requested.

IX. APPENDICES

The first attached Appendix contains a copy of the claims on appeal.

The second and third Appendices have been included to comply with statutory requirements.

No additional fees should be due for this Brief. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via electronic filing on July 25, 2007.

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Claims Appendix

Claim 1 (Finally Rejected) A system comprising:

a first node that includes an ordering point for data, the first node being operative to employ a write-back transaction associated with writing the data back to memory, the first node broadcasting a write-back message to at least one other node in the system in response to an acknowledgement provided by the memory indicating that the ordering point for the data has migrated from the first node to the memory.

Claim 2 (Finally Rejected) The system of claim 1, wherein the first node comprises a processor having an associated cache that comprises a plurality of cache lines, one of the plurality of cache lines having an associated state that defines the cache line as a cache ordering point for the data prior to employing the write-back transaction.

Claim 3 (Finally Rejected) The system of claim 1, wherein the at least one other node provides a response to the first node acknowledging receipt of the write-back message broadcast by the first node.

Claim 4 (Finally Rejected) The system of claim 3, wherein the first node maintains the write-back transaction active until the first node receives responses from the at least one other node to the write-back message broadcast by the first node.

Claim 5 (Finally Rejected) The system of claim 4, further comprising a third node that issues a source broadcast request for the data employing a source broadcast protocol, the third node retrying the source broadcast request for the data in response to recognizing a conflict associated with the source broadcast request for the data.

Claim 6 (Finally Rejected) The system of claim 5, wherein the conflict is recognized by the third node in response to one of (i) receiving the write-back message broadcast by the first node while the source-broadcast request for the data is active at the third node, or (ii) receiving a conflict response from the first node to the source broadcast request issued by the third node.

Claim 7 (Finally Rejected) The system of claim 5, wherein the third node retries the source broadcast request employing a forward progress protocol.

Claim 8 (Finally Rejected) The system of claim 1, wherein the first node further comprises a request engine having an associated miss address file, the request engine allocating an entry in the miss address file associated with the write-back transaction for the data that is maintained in the miss address file until responses have been received from all other nodes in the system to the write-back message broadcast by the first node.

Claim 9 (Finally Rejected) A computer system, comprising:

a first processor that provides a write-back request to transfer an ordering point for desired data from associated cache of the first processor to memory;

the memory providing an acknowledgement back to the first processor in response to the write-back request, the first processor providing a source broadcast write-back request to the system in response to the acknowledgement provided by the memory; and

at least one other processor in the system that provides an acknowledgement response to the first processor in response to the source broadcast write-back request provided by the first processor.

Claim 10 (Finally Rejected) The system of claim 9, wherein the system employs a source broadcast protocol, the system further comprising a third node that issues a source broadcast request for the desired data, the third node

reissuing the request in response to recognizing a conflict associated with the source broadcast request for the desired data.

Claim 11 (Finally Rejected) The system of claim 10, wherein the conflict is recognized by the third node in response to one of (i) receiving the source broadcast write-back request provided by the first node while the source-broadcast request for the desired data is active at the third node, or (ii) receiving a conflict response from the first node to the source broadcast request issued by the third node.

Claim 12 (Finally Rejected) The system of claim 10, wherein the third node reissues the request employing a forward progress protocol implemented in the system.

Claim 13 (Finally Rejected) The system of claim 9, further comprising an entry in a miss address file at the first processor that is associated with transferring the ordering point from the associated cache of the first processor to the memory, the entry in the miss address file being maintained until responses to the source broadcast write-back request have been received from all other processors in the system.

Claim 14 (Finally Rejected) The system of claim 9, wherein the first processor comprises a cache line that contains the desired data in a state that defines the cache line as the ordering point for the desired data prior to issuing the write-back request to the memory.

Claim 15 (Finally Rejected) The system of claim 14, wherein the state that defines the cache line as the ordering point for the desired data is selected from a group consisting of a modified state, an owner state and a dirty state, the cache line transitioning to an invalid state after issuing the write-back request to the memory.

Claim 16 (Finally Rejected) A multiprocessor computer system, comprising:

means for issuing a write-back request to migrate an ordering point for data from an associated cache to memory; and

means for providing a source broadcast write-back message associated with the data to the system in response to the memory acknowledging receipt of the write-back request.

Claim 17 (Finally Rejected) The system of claim 16, further comprising means at each of at least one node in the system for acknowledging receipt of the source broadcast write-back message.

Claim 18 (Finally Rejected) The system of claim 17, further comprising means for retiring an outstanding transaction associated with migration of the ordering point to the memory from the associated cache in response to receiving acknowledgement of receipt of the source broadcast write-back message.

Claim 19 (Finally Rejected) The system of claim 16, further comprising means for recognizing a conflict associated with the data.

Claim 20 (Finally Rejected) The system of claim 16, wherein the means for issuing the write-back request comprises a first processor including a cache line that contains the data in a state that defines the cache line as the ordering point for the data prior to migration of the ordering point to the memory.

Claim 21 (Finally Rejected) The system of claim 20, wherein the state that defines the cache line as the ordering point for the data is selected from a group consisting of a modified state, an owner state and a dirty state, the cache line

transitioning to an invalid state after issuing the write-back request to the memory.

Claim 22 (Finally Rejected) The system of claim 16, further comprising means for transitioning a cache line in the associated cache to an invalid cache state for the data after the write-back request is issued.

Claim 23 (Finally Rejected) A method comprising:

providing a write-back request from a first processor node to transfer an ordering point associated with data to memory;

acknowledging receipt of the write back request at the memory; and

issuing a source broadcast message from the first processor node to other nodes in response to the acknowledging receipt of the write back request at the memory.

Claim 24 (Finally Rejected) The method of claim 23, further comprising providing a response from each of the other nodes to acknowledge receipt of the source broadcast message at the other nodes.

Claim 25 (Finally Rejected) The method of claim 24, further comprising maintaining a write-back transaction at the first processor node until the first

processor node receives the responses to the source broadcast message from the other nodes.

Claim 26 (Finally Rejected) The method of claim 25, further comprising retiring the write-back transaction at the first processor node in response to receiving the responses from each of the other nodes acknowledging receipt of the source broadcast message.

Claim 27 (Finally Rejected) The method of claim 23, further comprising recognizing a conflict associated with a request for the data provided by at least one of the other nodes.

Claim 28 (Finally Rejected) The method of claim 27, wherein the request for the data provided by the at least one of the other nodes comprises a source broadcast request, the recognizing of the conflict further comprising recognizing the conflict in response to one of (i) receiving the source broadcast write-back request provided by the first processor node while the source-broadcast request for the data is outstanding at the at least one of the other nodes, or (ii) receiving a conflict response from the first node to a source broadcast request issued by the at least one of the other nodes.

Claim 29 (Finally Rejected) The method of claim 23, wherein the first processor comprises a cache line that contains the data in a state that defines the cache line as the ordering point for the data prior to issuing the write-back request to the memory.

Claim 30 (Finally Rejected) The method of claim 29, further comprising transitioning the state of the data in the first processor from a first state to an invalid state after issuing the write-back request to the memory, the first state being selected from a group consisting of a modified state, an owner state and a dirty state.

Evidence Appendix

None

Related Proceedings Appendix

None